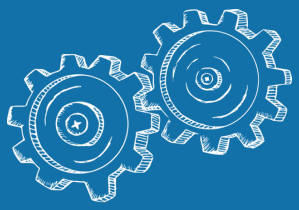


Reverse-Engineering and Side Channel Evaluation on Memory Access Latencies

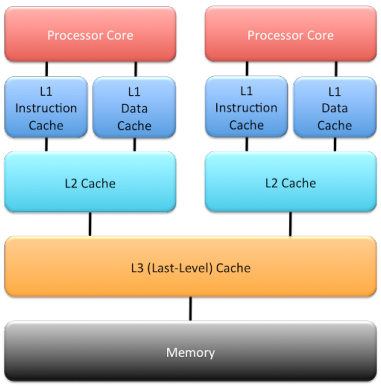
Advisor: **Carina Fiedler**

Motivation

Memory accesses exhibit different access latencies depending on a variety of factors: e.g., the cache level they reside in, whether the address translation is cached, or due to contention in the DRAM bank. We observed a timing difference for certain addresses that does not fit any of these known categories. The goal of this thesis is to explore and evaluate this effect in detail.

Goals and Tasks

- Get familiar with timing side channel evaluation methods such as covert channel construction.
- Perform experiments to narrow down the source of this contention effect and evaluate under which conditions it occurs.
- Implement an attack to leak information from a victim.
- Form a hypothesis about possible underlying microarchitectural structures.



Literature

Courses & Deliverables

- ☑ **Introduction to Scientific Working**
  Short report on background
  Short presentation
- ☑ **Bachelor Project**
  Project code and documentation
- ☑ **Bachelor's Thesis**
  Project code
  Thesis
  Final presentation

Recommended if you're studying

☑ CS ☑ ICE ☑ SEM

Prerequisites

- Interest in the timing side channels/microarchitecture
- OS, SCS may be beneficial (basic knowledge of address translation, caching, timing side channels)
- Programming (C++)

Advisor Contact

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