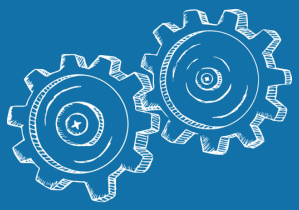

Exploring VexRiscv Core for Prototyping

Advisor: **Paul Gollob**

Motivation

The open-source RISC-V ecosystem offers many CPU designs for research and teaching. One interesting option is the *VexRiscv* core, written in SpinalHDL. It is a small, configurable, and **embedded-class** processor that can run bare-metal software without an operating system. The core also supports an MMU configuartion to support 32-bit virtual memory. Its modular structure makes it easy to understand and extend, which could be useful for system security research and prototyping.

In this bachelor project, you will explore whether VexRiscv and SpinalHDL are suitable tools for security-oriented hardware prototyping. Possible directions include testing the hardware design flow, adding simple security extensions, or evaluating how easy it is to adapt the CPU for our research needs.

This project is ideal for students interested in computer architecture, embedded systems, or hardware security, and who want practical experience with open-source RISC-V hardware.

Goals and Tasks

- Get familiar basic layout of an embedded CPU architecture with MMU support.
- Explore SpinalHDL as a modern, high-level hardware description language.
- Implement small known system security features.
- Evaluate if the core is useful for prototyping in system security.

Literature

- S. contributors
  VexRiscv: A FPGA-friendly 32-bit RISC-V CPU implementation
  https://github.com/SpinalHDL/VexRiscv
- C. Papon and Y. Xiao
  SpinalHDL
  https://github.com/SpinalHDL/SpinalHDL

Courses & Deliverables

- ☑ **Introduction to Scientific Working**
  Short report on background
  Short presentation
- ☑ **Bachelor Project**
  Project code and documentation
- ☑ **Bachelor's Thesis**
  Project code
  Thesis
  Final presentation

Recommended if you're studying

☑ CS ☑ ICE ☑ SEM

Prerequisites

- Basic knowledge of CPU architectures and HDL (Verilog or VHDL ...)
- CON, InfoSec

Advisor Contact

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